Printed Circuit Board Layout Time Estimation

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ABSTRACT

System design complexity is growing rapidly. As a result, current development costs can be staggering and are constantly increasing. As designers produce ever larger and more complex systems, it is becoming increasingly difficult to estimate how much time it will take to design and verify these designs. To compound this problem, system design cost estimation still does not have a quantitative approach. Although designing a system is very resource consuming, there is little work invested in measuring, understanding, and estimating the effort required.

To address part of the current shortcomings, this paper introduces $\mu PCBComplexity$, a methodology to measure and estimate PCB (printed circuit board) design effort. PCBs are the central component of any system and can require large amounts of resources to properly design and verify. $\mu PCBComplexity$ consists of two main parts, a procedure to account for the contributions of the different elements in the design, which is coupled with a non-linear statistical regression of experimental measures. We use $\mu PCBComplexity$ to evaluate a series of design effort estimators on several PCB designs. By using the proposed $\mu PCBComplexity$ metric, designers can estimate PCB design effort.

1 Introduction

Printed circuit board (PCB) design effort keeps growing as additional constraints such as rising clock frequencies, reduced area, increasing number of layers, mixed signal devices, and the ever increase in component numbers and densities. All of these factors combined have led to a steady rate of increase in development costs for current systems. As we design ever larger, denser and more complex systems, it is becoming increasingly difficult to estimate how much time would be required to design and verify them. To compound this problem, PCB design effort estimation still does not have a quantitative approach. We present in this paper a first step toward creating a design effort metric that is highly correlated with design effort for PCB layout. We follow the same approach taken in [1] as the principles that are applicable to microprocessors are also applicable to PCBs. In this paper, design effort corresponds to the number of engineering-hours required for implementation (layout) of a PCB design.

This paper analyzes and proposes various statistics to estimate the layout effort required to develop PCBs. We investigate and quantify statistics such as area, component count, pin count and device types and sizes for many PCBs. We analyze several of these statistics, and propose a metric, obtained after applying non-linear regression over the different statistics, which we call $\mu PCBComplexity$. In addition, we provide insights on the correlation between several statistics and design effort for several known layout design times.

Different designs have different constraints, leading to specific challenges; typical design constraints being area, frequency, and cost. For example, having area being a primary design constraint, may lead to a requirement for additional layers, more expensive package types, and more complex placement and routing. A design constrained by cost, on the other hand, may require a balance between number of layers, area, drill density, types of packages and possibly the number of different drill sizes. Having clear constraints is necessary in estimating layout effort as it can drastically affect complexity.

We define design effort to be the layout time required by one engineer. Design effort is equivalent to layout time when the project has a single developer, which is frequent even for complex PCBs. Nevertheless, for a given effort requirement, it is possible to reduce the design time by increasing the number of workers. Nevertheless, increasing the number of workers decreases the productivity per worker. The relationship between these two elements has been widely studied in software metrics and business models. Since the conversion between design effort and design time can be approximated, the remainder of this paper focuses only on design effort.

The rest of the paper is organized as follows. Section 2 covers other work in this area; Section 3 describes the statistical techniques that allow us to calibrate and evaluate the $\mu PCBComplexity$ regression model; Section 4 describes the setup for our evaluation; Section 5 evaluates several statistics for the boards in our analysis; and Section 6 presents conclusions and future work.

2 Related Work

The capability to rapidly develop complex PCBs is a tremendous competitive advantage, since high development productivity is essential for the success of any design team. Although some companies have used statistical methods to estimate PCB design time, those methods are considered trade secrets [9]. Other companies do not release details because

they provide competitive advantage over other companies. As a result, we are unaware of any published work on the topic of predicting the engineering hours required for a PCB design.

[1] focuses on microprocessor design effort. While the work described in this paper focuses on PCB design metrics, [1] uses the same regression model, but both papers analyze different set of statistics and targets.

Another paper that looks at productivity is [7] which identifies the need for standards or infrastructures for measuring and recording the semiconductor design process. They propose improving design technology, time-to-market, and quality-of-result by addressing the Design Productivity Gap and the Design "Technology" Productivity Gap. However, this previous work focused mostly on the problems associated with the infrastructure and design tools related to the physical implementation of semiconductor designs, while the focus of this paper is layout effort associated with PCB designs.

In [8] a factor similar to the productivity factor is described. They use the "process productivity parameter" to tune the estimating process for software projects. They contend that if you know the size, time, and the process productivity parameter you can use it to make estimates for a new project. So long as the environment, tools, methods, practices, and skills of the people have not changed dramatically from one project to the next.

Much research has been done in Design for Manufacturing (DFM) and Design for Production (DFP) which seek to improve the production and manufacturing times of PCB assemblies. This paper seeks to develop a metric that can aid in predicting the layout effort, based on analysis of characteristics of PCBs at a low-level so as to better plan for future generations of systems. In [2] the issue of embedded passive components is discussed as a necessity to the smaller electronic devices requiring ever smaller PCBs. They note that board area is becoming so critical that to keep pace with the size constraints new techniques are required. Our goal would be to eventually develop a set of metrics and a model that estimates design effort by also taking into account manufacturing times.

3 Approach

Our goal is to develop a quantitative approach and to have a model that quickly estimates design effort based on several easily gathered statistics. This is important because being able to predict design effort is advantageous in helping to reduce design costs. To build the model, we analyze many commercial computer/electronic devices and gather data from the PCBs within. The layout times for these PCBs were well documented which was a requirement for this analysis. Table 1 lists the critical components of PCB designs as determined by [2]. These parameters contribute to the complexity of a design, and hence the time required to do layout.

Some design parameters listed in Table 1 are dependent on other factors. For example, the size of the board is defined by the number of embedded and discrete passive components and

1.	Board dimensions (length and breadth)
2.	Total wiring requirements
3.	Number of layers
4.	Number of embedded resistors (if used)
5.	Number of embedded capacitors (if used)
6.	Set of active component types and their number
7.	Thickness of the board
8.	Number of discrete resistors
9.	Number of discrete capacitors

Table 1: Critical design parameters for a PCB.

total wiring requirements. However, the total wiring requirements are governed by the number of embedded and discrete passive components in the PCB. And further more, the total number of layers in the PCB depends on the size of the board, the number of embedded and discrete resistors and bypass capacitors [2].

These critical design parameters are focused towards manufacturability, not design effort estimation. We used them as a starting point in determining what parameters or metrics to analyze and include for correlation with design effort. None of the boards in our study have embedded passive components, instead we focus on the total number of all components (passive and discrete) and the pin count for them. These are easily obtainable values.

Since the routing data is not easily obtainable, the number of pins for all the components in the design are taken into account instead. While this is not an ideal metric since not all pins are used or have very short traces (VDD or GND), it is readily obtainable an does not hamper the focus of this paper, namely effort prediction starting from higher level design descriptions, such as a bill of materials (BOM) or schematics.

In order to find a metric highly correlated with design effort, several statistics were gathered from the existing designs. For each isolated board with a known design effort, we look at several statistics and apply non-linear regression to find a highly correlated metric.

We present our design effort model as the aggregate of a set of statistics (S_i). Each of which has a specific constant (w_i), associated with it, which assigns a weight to the importance of every statistic used as input in the model. The aggregate of the statistics is inversely proportional to the productivity of a specific design team which is represented by a constant (ρ). The model is presented in Equation 1. In order to find suitable values for each of the data weights (w_i) we perform mixed non-linear regressions on this equation. The design team productivity factor (ρ) is constant per design group, and it needs to be adjusted on a per company or design team basis. If the ρ is unknown, then the absolute design effort is invalid and only the breakdown inside the project is correct. Obtaining the value of ρ is simple; all that is needed is to have the design effort for a single project. Alternatively, it is possible to develop a productivity benchmark suite that calibrates ρ for a given company.

$$\text{Design Effort} = \frac{1}{\rho} \times \sum_{k=1}^{n} (w_k \times S_k) \qquad (1)$$

In order to determine the weights that give a generalized solution to Equation 1, [1] proposes to use a mixed non-linear regression model. If there are no productivity adjustments, it is possible to use a simpler non-linear regression model. While the sum of a large number of random variables is distributed normally, the product of a number of random variables is distributed *lognormally* — a distribution where the logarithm of the variable is normally distributed [4]. Therefore, since the random variables have a log normal distribution an even simpler linear regression model can not be used.

To evaluate the accuracy of the model (Section 5), we use σ as a measure of error associated with the fit. Consequently, it is important to understand what different values of σ tell us about the quality of the estimate. For a given σ, we can find a *confidence interval* for the estimated effort. The x% confidence interval for a metric is defined to be the range of efforts ($Estimate_{low}, Estimate_{high}$) such that $P(Estimate_{low} < \text{metric prediction} < Estimate_{high}) = x/100$. For example, the 90% confidence interval gives us two values a and b such that there is a 90% chance that the actual effort is between metric prediction $\times a$ and metric prediction $\times b$.

3.1 Productivity Adjustments

In software development projects, it is well known that different development teams have different productivities. For example, it has been shown that the productivity difference between teams can be up to an order of magnitude [5]. We believe that a similar effect occurs between PCB design teams. The productivity differences may be due to multiple factors, including the average experience of the designers in the team and the tools used. In our model, ρ captures this effect.

The boards under study in this analysis all come from one manufacturer and so the use of a productivity factor was not necessary.

3.2 Team Size Dynamics

Although some board designs require long periods of time, it is very rare to find multiple developers doing different sections of the same board. The PCB layout effort by nature is a linear task done by one engineer at a time. To reduce the design time, we have found two approaches: multi-timezone working environments, and "surgical" teams.

A multi-timezone team has different designers working on multiple time zones, this is, once a designer stops working a new designer can continue and pick up where the previous designer left. A "surgical team" [6] follows an alternative design organization, with the surgeon, or chief designer, at the helm and a supporting staff that has their tasks allocated by the chief of staff. In the PCB case, we may have other designers doing such tasks as making footprint images for components, which can be a tedious effort.

3.3 R-Language

This section provides the R-language [10] code to fit the non-linear mixed-effects model and the non-linear regression model. The mixed-effects model is needed when productivity adjustments (ρ) are required, a simpler model is used when no productivity adjustments are required.

Recall that our model has a multiplicative lognormal error and also a lognormal distribution for the random effect ρ. Simply taking the logarithm of both sides of the equation gives us the requisite additive normal error and normal random effect as follows. Hence the need for a non-linear model.

```
# mixed-effects non-linear model
nlme(model=log(Effort) ~
  (log_rho) + log(w1*stat1 + w2*stat2)
  ,random = log_rho ~ 1 | team
  ,fixed  = list(w1 ~ 1, w2 ~ 1)
  ,start = c(0.1, 0.1)
  ,data=(traw)
  ,method="ML")

# non-linear model
nls(log(Effort) ~
  log(w1*stat1 + w2*stat2)
  ,start=list(w1=0.1,w2=0.1)
  ,data=traw)
```

The R-language is also used to compute the confidence intervals. To obtain a 90% confidence interval for a given σ (s) generated, the following R-language code $c(exp(s * qnorm(0.05)), exp(s * qnorm(0.95)))$ is used.

4 Evaluation Setup

We gathered data from a number of PCB designs for the analysis done in this paper. Table 3 shows the types of statistics gathered for each of the boards analyzed. When calculating the area consumed for each component we did not consider the cases where routing, or in the more rare case placement, could be done underneath a component. Several board designers pointed out that the component and pin density of the board was one of the crucial factors to estimating design effort. To capture component and pin density, we define them with equation 2 and equation 3 respectively.

$$\text{Component Density} = \frac{\# \text{ Components}}{\text{PCB Area} \times \# \text{ Sides w/ components}} \qquad (2)$$

$$\text{Pin Density} = \frac{\# \text{ Pins}}{(\text{PCB Area})} \qquad (3)$$

Table 2 gives a description of the boards along with the engineering notes that we were able to gather from the designers. Boards B7-B11 used SPECCTRA for OrCAD which is a common autorouter used in industry. No data was available on the use of an autorouter for boards B1-B6 but it can be safely assumed that some autoroute tool was used.

In discussions with the designer of boards B8 and B9 the size of the LCD in the system dictated the size of the PCB and the housing that contained it. The LCD was counted as a

Board	Description	Engineering Notes
B1	Signal Conditioning	Many thru-hole components. Analog board with many important signal paths
B2	AE RMS	Many thru-hole components. Analog board with many important signal paths
B3	PMD Motor Controller	Many high density components
B4	Motor Driver	New footprints
B5	Enviro Controller	Forgot reasons why it took so long
B6	Current Source	Many components on a small board. Mechanical constraints
B7	Arbitrary Waveform Generator/Amplifier	Placement constraints due to noise reduction
B8	ACDC Monitor	Cost major factor. Time consuming to keep to a 2 layer board
B9	Tank Monitor	Cost major factor. Time consuming to keep to a 2 layer board
B10	Air spring remote	Very small. RF constraints
B11	Air Spring Controller	2 Isolated grounds with placement constraints

Table 2: Description of boards analyzed.

Board Statistic	Description
PCB Size (mm^2)	Physical size of the PCB
# of Sides w/ Comp	Either 1 or 2 sides has components
# of Routing Layers	Layers used for routing traces
# of Layers	The total number of layers in the PCB
Components	
# Passive	Passive components (resistors. . .)
# Digital	Digital integrated circuits (IC)
# Analog	Analog ICs or devices (opamps. . .)
# Mixed Signal	ICs with both digital and analog sections
Total #	Total count of all components on PCB
Total Area (mm^2)	Total area of all components on PCB
Density	Ratio of component area to area
Pins	
# Passive	Pins for all passive components
# Digital	Pins for all digital components
# Analog	Pins for all analog components
# Mixed Signal	Pins for all mixed signal components
Total	Pins for all devices on PCB
Density	Ratio of number of pins to area

Table 3: Description of the statistics gathered from the PCBs.

component in our analysis and took one complete side of both these boards, forcing the placement and routing of all other components to one side. Cost was the main consideration for both these boards also and this forced the designer to route everything using only 2 layers.

Among boards B7 through B11 the smallest board, B10, was judged to be the most difficult to layout. Where as boards B7 and B11 were the easiest. This was attributed to the areas available to do the placement and routing. B7 and B11 were two of the largest boards reviewed and they were not area constrained, this gives much latitude to the designer for placement and makes the autorouter produce better results. With a more constrained area more human intervention is required during the routing phase which was the case for B10.

For the placement stage we only had to consider the number of sides of the board on which components were mounted. Most of the boards in this study had the components all on one side, though a few had bypass capacitors mounted on one side, which accounted for a negligible amount of space. Again, thru-hole devices would effect the available placement area as it did the available routing area as space would be lost on both sides of the board, unlike with surface mounted components. This was not a factor in this study since most boards only used one side for placement. Boards B8 and B9 had components on both sides but one side was populated by only one component,

the LCD. Board B10, the only other board with components on both sides, did not have any thru-hole devices present.

5 Evaluation

Our evaluation analyzes 11 different printed circuit boards. Table 4 shows the main results and characteristics for each of these. The first column corresponds to each of the statistics or metrics presented in Table 3 (Section 4). Columns B1 to B11 correspond to each of the boards (Table 2). The last column corresponds to the σ between the row and design effort. Since all the boards are designed by the same team, we do not evaluate the productivity factor (ρ). This simplifies the analysis, and we can use non-linear regression instead of the mixed-effects non-linear regression model. With σ we can compute the confidence interval. For the lognormal distribution used, the mapping between σ and the 90% confidence interval is shown in Figure 1. We will use this chart to compare the accuracy of different estimators.
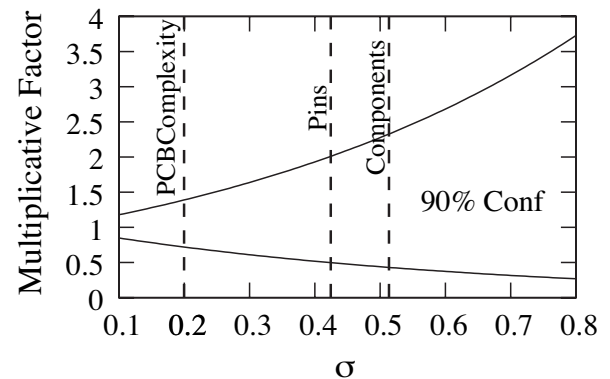

Figure 1: Mapping between the standard deviation of the error (σ) and the 90% confidence interval for the lognormal error distribution used.

The design effort values were obtained by interviewing the original designers. Obviously, there is perfect correlation with itself so $\sigma = 0$. A zero σ results in a perfect $(1, 1)$ confidence interval. We now proceed to analyze easily available statistics like number of components and pin count. These two sets of statistics are easily available before the PCB design starts. They are part of the PCB specification.

From the boards analyzed, we observe that it is best to

	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	σ
Design Effort (hours)	68	35	43	21	48	48	24	40	32	24	12	0
Components												
# Passive	213	165	101	80	108	222	116	86	83	19	47	0.52
# Digital	15	0	17	0	8	2	0	11	8	4	4	0.99
# Analog	24	24	1	10	24	50	28	4	16	1	11	1.10
# Mixed Signal	11	0	7	0	0	3	0	0	0	0	0	0.75
Total #	263	189	126	90	140	277	144	101	107	24	62	0.51
Total Area (mm2)	6214	9053	6964	2719	9144	6579	8104	12193	12296	777	5430	0.93
Pins												
Passive	563	429	365	182	414	578	414	194	188	39	109	0.62
Digital	154	0	518	0	107	32	0	175	173	88	32	2.18
Analog	188	208	8	98	72	400	150	25	53	14	65	1.19
Mixed Signal	172	0	208	0	0	48	0	0	0	0	0	2.00
Total	1077	637	1099	280	593	1058	564	394	414	141	206	0.43
PCB Size (mm2)	22194	22194	22194	16258	38710	20452	22194	10968	10968	1277	25548	0.52
# of Sides w/ Comp	1	1	1	1	1	1	1	2	2	2	1	3.17
# of Routing Layers	2	2	3	2	2	2	3	2	2	4	2	1.18
# of Layers	4	4	6	4	4	4	4	2	2	4	2	0.94
Component Density (x1000)	62	45	30	29	19	71	34	24	26	49	13	0.48
Pin Density	50	30	51	18	16	54	26	37	39	115	8	0.64
$\mu PCBComplexity$ (hours)	60	44	44	16	37	57	32	35	33	24	13	0.2

Table 4: Statistics, design effort, and correlation results of study boards.

use the total number of components to estimate design effort ($\sigma = 0.51$). Although traces for analog components and digital components are more difficult than traces for passive components, the low amount of digital and/or analog components on several of the boards make it difficult to use them as a method to estimate effort. Figure 1 shows the confidence interval for a $\sigma = 0.51$ as the intersection between the components line and the confidence interval line $(0.43, 2.31)$. This means that using the number of components on the specification, we have a 90% confidence that the design effort would be between 0.43 and 2.31 times the prediction.

Statistics about the pins are as easily available as components even before the design starts. The number of pins is an even better predictor ($\sigma = 0.43$) than the number of components ($\sigma = 0.51$). The resulting 90% confidence interval for the number of pins is $(0.49, 2.03)$. This means that just by using the pins, we have a 90% confidence that the prediction is roughly half or double the expected design effort. Not shown in the table is the result of combining the number of pins and the components to predict design effort. The results did not improve because there is a high correlation between pins and components.

Area is an interesting statistic. Just by knowing the final dimension of the board, we can estimate design effort with a $(0.43, 2.35)$ confidence interval. This is roughly the same accuracy as the number of components. The reason is that PCBs are always area constrained [1]. If the specification provides a realistic area constraint, it could be a good way to estimate design effort. Table 4 also shows other statistics such as number of sides used, routing layers, and number of layers. Those statistics are not so useful by themselves because they are highly quantized, and this makes them difficult to use to predict effort.

The proposed $\mu PCBComplexity$ metrics are now evaluated.

[1] Bigger PCBs have higher cost.

To obtain $\mu PCBComplexity$ shown in Table 4, we analyzed multiple combinations of parameters and followed suggestions from experienced board designers. The best results were achieved when using the following equation:

$$\text{Effort} \propto \text{\# Passive Comp.} + \text{Comp. Density} + \text{Pin Density} \tag{4}$$

Section 4 explains how to compute component density and pin density. To obtain the factors on equation 4, we perform non-linear regression as explained in Section 3. Although neither pin nor component density can achieve better predictions than the number of pins, when integrated together in the $\mu PCBComplexity$ metric we achieve a 0.2 σ. As Figure 1 shows, this represents a $(0.72, 1.39)$ confidence interval. This roughly means that by using the proposed $\mu PCBComplexity$ metrics, with a 90% confidence designers can predict design effort with less than 40% error.

Figure 2 shows a scatter-gather plot between design effort and our $\mu PCBComplexity$ metric. This is an intuitive way to see that there is a high correlation between design effort and the metric proposed.

$\mu PCBComplexity$ works well because PCB design complexity increases as the component and pin density increases. Designers can increase the number of layers on the PCB to decrease the pin density or increase the area to reduce both densities. The problem is that both approaches require more costly boards. As a result, designers trade-off between time to market and density.

6 Conclusions & Future Work

The goal of this paper was to explore the correlation of some easily obtained metrics of a PCB and see which were most correlated to the design effort required during the layout stage of development. Many simplifications were made; we did not
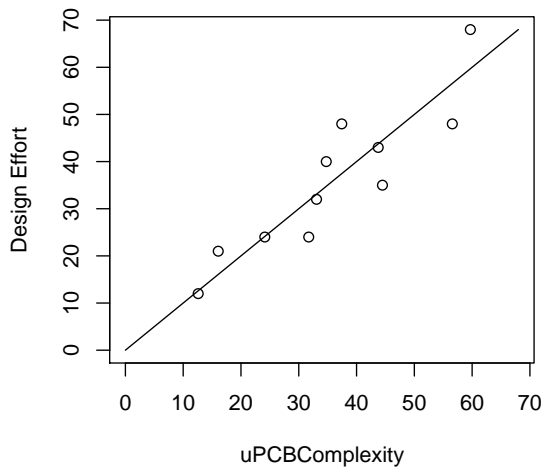
Figure 2: Scatter-gather plot of design effort vs. PCB metric

account for traces of differing sizes, we did not look at hole sizes or density, the frequency of the boards were not considered, nor the extra considerations required for analog noise filtering. Also, we need additional PCBs from more companies with teams of differing sizes to develop a more general model for predicting design effort.

Many factors and constraints effect the design effort required for a board to be successfully placed and routed. Some difficulty metric would be helpful but guidelines need to be established as difficulty is a very subjective term. Being able to analysis different options for a board would be useful, such as being able to change the size of the board to see what effect it would have on the estimated design effort. This could be expanded to also include the number of layers since this would ease routing congestion.

We see this initial research leading into more areas of study in PCB design optimization and analysis. We are currently analyzing data from additional PCB designs from different sources. These new designs have more components, more layers, higher frequencies, and more power plains. This will give us additional metrics to add to our model for possible better correlation to design effort. These designs also have more designers on the team which will necessitate some team or company productivity factor.

We have extended the previously proposed $\mu Complexity$ models [1] to the PCB domain. We plan to apply the model to a number of classes at UCSC that do board development to give design guidelines to students and further refine our approach. Our model and metrics will eventually be available to researchers and industry for use in scheduling and planning PCB projects.

The evaluation shows that a simple statistics like PCB area size and number of components yield some correlation with design effort. With a 90% confidence, area has a (0.43

2.35) confidence interval. This means that roughly by looking at any of those statistics the typical design time error is half/double with a 90% confidence. Much better results can be achieved with the proposed $\mu PCBComplexity$ metric. In that case the confidence interval for a 90% confidence is (0.72 1.39). This roughly means that less than 40% estimation error is done with a 90% confidence.

Despite the good results, we still believe that much work needs to be done in gathering relevant designs to evaluate (with associated known design times) and to refine the metrics and models. A major goal would be a rule of thumb type equation that given some easily obtainable design parameters an accurate estimator of design time would be generated.

Acknowledgments

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