# SOI, Interconnect, Package, and Mainboard Thermal Characterization

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## ABSTRACT

This paper presents an evaluation to determine the importance of the accurate thermal characterization for several elements of a semiconductor device. Specifically, it evaluates whether the decision to simplify or neglect to model metal interconnect density variation, Silicon-On-Insulator technology, the chip package, or the system main-board can effect the overall accuracy of a thermal model. In performing this evaluation, we motivate the need for more accurate thermal characterization of semiconductor devices. Through this analysis, designers are better able to understand how simplifications to their temperature models can effect the validity of design decisions derived from such models.

To perform this evaluation, a novel temperature modeling infrastructure was designed that offers engineers a new way to explore solutions to a growing array of engineering problems that require accurate thermal characterization of semiconductor devices. The modeling framework, called SESCTherm, is a state-of-the-art finite-difference-based thermal modeling system.

## Categories and Subject Descriptors

C.4 [**Performance of Systems**]: Modeling Techniques

## General Terms

Design and Verification

## Keywords

Thermal Modeling, Package Modeling, SOI Modeling, Interconnect Modeling

## 1. INTRODUCTION

Due to dramatic refinements in fabrication and process technologies, the transistor density of chips is constantly increasing with each technology generation. There is a direct correlation between transistor density and power density/temperature.


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Increases in temperature influence chip reliability, performance, and leakage power consumption. Specifically, power density impacts chip reliability through electro-migration and dielectric gate breakdown. Performance is sacrificed to mitigate these effects and to prevent the device from overheating. Leakage is exponentially dependent on temperature. [1]

To address these concerns, a variety of temperature modeling frameworks have been developed to assist engineers in characterizing their desings. However, there is no comprehensive analysis that accurately models various elements of the thermal system for a chip, the associated package, and system main-board. Specifically, to our knowledge there is no comprehensive quantitative approach to evaluate the transient thermal accuracy of a thermal model infrastructure that takes into account interconnect density variation, silicon-on-insulator technology (SOI), and detailed materials modeling for the package and main-board.

Since temperature is such an important factor in current and future chip designs, this paper analyzes the importance and impact of SOI modeling, transitor and metal lines densities, chip package, and main-board. To do so, we introduce SESCTherm, a novel temperature modeling infrastructure based on finite-difference analysis techniques. SESCTherm is verified, for both steady-state and transient cases, against empirical data collected using a thermal test chip, and the Flomerics Flotherm$^{TM}$ thermal simulator.

The rest of the paper is organized as follows. Section 2 describes the theoretical background behind the development of the proposed infrastructure; Section 3 describes the various material models developed; Section 4 evaluates the need for accurate thermal modeling of the non-uniform interconnect distribution, Silicon-On-Insulator technology, package, and system mainboard; Section 5 covers related work; and Section 6 presents conclusions.

## 2. SESCTHERM INFRASTRUCTURE

At the core of SESCTherm is a "finite-difference" model (FEM). Finite-difference analysis involves taking a problem and segmenting the problem into smaller pieces. SESCTherm divides the chip, package and associated components into a series of regular cross-sectional regions. Each region is a quadrilateral, and no two cross-sectional regions have abutting sides that are of different height or length. Each cross-sectional region is called a temperature "node", and each region has a series of properties. To accurately characterize complex materials and dimensions, SESCTherm subdivides regions by material and geometry. This means that each temperature node is considered to be one material or approximation of

[1] Although leakage is exponentially dependent on temperature, the quadratic component dominates for current technologies.

a combination of materials. Further, this means that any irregular shape is approximated by a combination of quadrilateral regions.

Each node of a thermal system can be considered either a heat source, heat sink, thermal capacitance, or thermal resistance. SESCTherm also updates the material properties as the temperature changes. The thermal conduction is solved similarly to the grid model from HotSpot [1]. In addition, SESCTherm also implements a convection model that involves heat transfer in a fluid. The transfer of heat in this phase of matter is dominated by the movement of molecules, rather than inter-molecular forces due to the weaker inter-molecular attraction in fluids.

SESCTherm has three discrete parts. The first part is a finite-difference modeling framework. The second part is a thermal modeling framework. The third part is a material modeling framework. To model temperature dependent material properties, SESCTherm updates material properties periodically based upon temperature fluctuations.

This paper focuses the various sub-models that make up the metal interconnect model, Silicon-On-Insulator model, package model, and main-board model. The models are activated and de-activated throughout this study to determine the impact upon the overall accuracy of the model.

# 3. MATERIALS MODELS

This paper proposes and evalutes models for accurate interconnect layer (Section 3.1), package and mainboard models (Section 3.2), and bulk silicon vs silicon-on-insulator (Section 3.3).

## 3.1 Interconnect Model

The flow of the interconnect model works as follows. First, a stochastic model is used for the purpose of distributing the various interconnects of various lengths across all of the metal layers. Second, a simplified heuristic is used to distribute the interconnects across each layer. Third, an electro-thermal model is used to characterize the lumped lateral and vertical thermal resistances of each floor-plan unit within each metal layer.

Heat flow is modeled laterally and vertically. Lateral heat flow is separately modeled both parallel and perpendicular to the routing direction of the interconnects. Density and specific heat computation is performed as a simple weighted average by mass of the density and specific heats of the respective materials within each modeling layer.

## 3.2 Package and Mainboard Model

The chip package is an important avenue for thermal optimization. The thermal conductivity of copper is 1000 times that of most polymers (BT, FR-4 and epoxy) that make up most package and mainboard interlayer dielectric layers. This means that the primary heat flow path through the interconnect layer stack of either the package or mainboard PCB is through the wiring traces. Further, this means that the chosen layout of the traces and the geometry of the traces themselves may have a significant impact upon the thermal performance of the interconnect layer stack.

The heat flow path through the main-board is dependent upon various factors including the density of thermal vias under the thermal landing pad of the package. Similar to the heat flow through the interconnect layers (Section 3.1), the vertical heat transfer path is a series resistance of the total heat flow path through the main-board layer stack. For each wiring layer, a lumped resistance is computed for the lateral and vertical thermal resistance. Similar to the package interconnect layers, the vertical heat transfer is a parallel resistance between the interlayer epoxy insulation and the copper vias. However the vias are modeled differently in this case. Unlike the chip and package vias, which assume that the via metal plating is the same as the radius of the via, the main-board vias have a plating thickness which can vary depending upon the manufacturing process.

The package model is hence a very similar structure to the main-board structure described elsewhere. SESCTherm relies largely upon the flip chip plastic ball grid array materal layer stack described by Ramakrishna et al. [2]. Four regions of the package are described. First, is the C4 solder balls and chip underfill that reside under the chip die. Second, is the package substrate which is placed under the solder ball region of the package. Third, a C5 layer is synthesized that simulates the thermal properties of the C5 solder balls. Lastly, the package printed wiring board (uPCB) is defined.

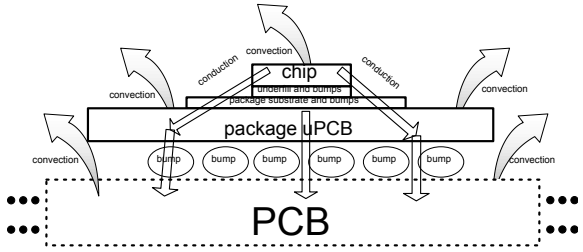


**Figure 1: General Heat Flow Path Through Chip, Package, and Mainboard.**

Under the package, SESCTherm includes a model for the main-board. As shown in Figure 1, the mainboard component consist of the package pins and a PCB thermal model like the uPCB but with longer and wider traces.

## 3.3 Bulk Silicon and Silicon-On-Insulator Transistor Layer Model

The transistor layer is designed to accurately represent the relevant lumped thermal characteristics of a bulk silicon technology process and Silicon-On-Insulator process. The flow is as follows. First, a transistor sub-model is used to determine lumped thermal characteristics of NMOS and PMOS transistor devices. Second, an interconnect sub-model is used to model lumped thermal characteristics of the poly-silicon interconnect and contact electrodes. Third, a simplified heuristic-based layout is used to distribute the transistors and interconnects across the chip. Using this simplified layout structure, a lumped electro-thermal model is created to derive lumped lateral and vertical thermal conductivities for each floor-plan unit.

For the Bulk silicon transistor sub-model, we model doped nwell regions and heavily doped p-well regions where $P^+$ or $N^+$ source/drain diffusion regions occur under the via contacts. In this model, we assume that the contact plugs are make of Tungsten. Further, a thin dielectric film is placed over the junction region – insulating a polysilicon ribbon from the underlying doped silicon substrate. Between the NMOS and PMOS transistor devices is electrical isolation either in the form of LOCOS ("Local Oxidation of Semiconductor") or STI ("shallow trench isolation"). A detailed discussion along with analytical expressions for the lateral and vertical thermal conductivities can be found in [3].

The SOI flow is very similar to that of the Bulk Silicon material model. First, a transistor sub-model is used to determine lumped thermal characteristics of the SOI transistor devices. Second, an interconnect sub-model is used to model lumped thermal characteristics of the poly-silicon interconnect and contact electrodes – including the silicon thin-film, field-oxide, and buried-oxide material layers. Third, a simplified heuristic-based layout is used to distribute the transistors and interconnects across the chip. From this, a lumped electro-thermal model is created to derive lumped lateral and vertical thermal conductivities for each floor-plan unit.

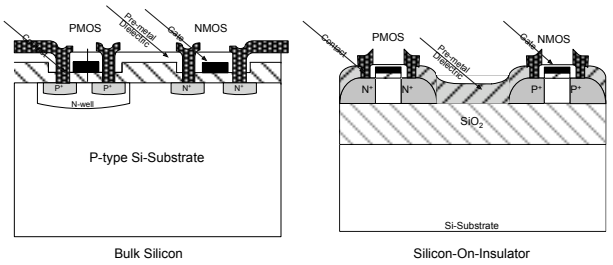


**Figure 2: Detailed electrothermal model design of transistor layer**

The thermal model in SESCTherm is based upon Semiconductor CMOS SOI, US Patent 6,975,003 [4]. As shown in Figure 2, the silicon-on-insulator device has a more complex geometry than the bulk-silicon MOSFET devices described previously. Specifically, each SOI MOSFET is etched into a thin layer of bulk silicon that is insulated from the rest of the silicon substrate through the use of a "buried-oxide" (BOX) layer of electrical insulation material. Further, STI (shallow trench isolated) is used to insulate adjacent transistors, where the deposition of an electrical insulator material surrounds each transistor.

This material model is a more accurate representation of the material distribution within the transistor layer of a silicon-on-insulator technology process than has been described in several other papers [5, 6]. In particular, previous approaches have modeled a simplified transistor geometry. It can be seen in Figure 2 that both NMOS and PMOS SOI transistor devices exhibit geometrical variations from the typical transistor device.

# 4. EVALUATION

Given the frequency with which thermal model simplifications are made, it is critical that designers fully understand the effect that neglecting certain modeling may have upon the validity of the conclusions drawn from such models. To address some of these concerns, SESCTherm is used to evaluate the need for accurately modeling various aspects of the thermal system. We systematically remove or change the thermal characterization of one or more components of the overall thermal model.

For the purpose of this investigation, we focus on four different components of the thermal system. First, we investigate the significance of modeling the variation in interconnect density within a given design. Second, we determine the significance of including an accurate thermal model for the chip package. Third, we investigate the significance of modeling Silicon-On-Insulator (SOI) technology versus Bulk silicon technology. Lastly, we evaluate the need to model the system mainboard. While there are clearly many more avenues of investigation, these components of the thermal model were chosen here because of their relative lack of discussion in the literature up to this point. In particular, little discussion has been placed upon the need for modeling of Silicon-On-Insulator technology versus Bulk silicon.

The chip modeled here is an AMD Mobile Athlon with a 754 socket. This chip was fabricated using a 130nm Silicon-On-Insulator technology process. A flip-chip pin-grid-array-based package is assumed.

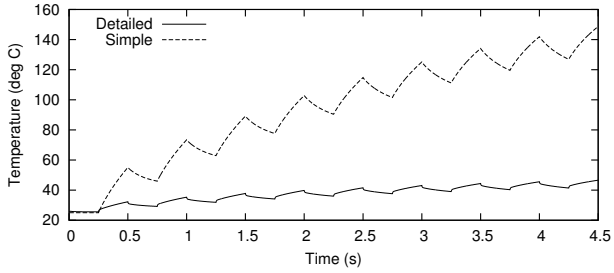


**Figure 3: Combined Error When Mainboard, Package, Interconnect Distribution and Silicon-On-Insulator Technology Are Not Modeled**

The combined effect of all of the simplifications can be seen in Figure 3. In this figure, the "Accurate" simulation accurately characterizes the thermal effects of the mainboard, package, non-uniform interconnect distribution, and Silicon-on-Insulator technology. The other, "Simple" plot neglects to model any of these elements. As can be seen, the effect on temperature is truly stunning. There is no difference in the cooling environment or input power trace in each of these cases. The temperature response of each of these systems is entirely different. While the "Accurate" simulation predicts a transient temperature response within a temperature range of 30°C to 40°C, the "Simple" thermal trace predicts thermal runaway, with a temperature rise quickly approaching 140°C.

It is important to separately determine the relative importance of accurately modeling each of the four components of the thermal system (mainboard, SOI, interconnect, package). To do this we separately compute the mean temperature error in °C of each component in Table 1 for two aspects of the temperature response of the model. First, we compute how neglecting to modeling these components will impact temperature fluctuations on a large time scale (4 seconds or more). This is shown in the first column (Default), which corresponds to the mean error for the thermal evolution of the model in Figure 3 over the first 4s . Second, we compute how inaccuracy in modeling these components will influence temperature fluctuations on a smaller time scale (1 second or less). This is shown in the second column (RC-Compensated), which shows the mean error once we compensate for the thermal runaway or long-term thermal RC time constant. These results indicate the mean error for the thermal evolution of the model in Figure 3 for each short-term temperature fluctuation of 1s or less.

Without RC-compensation, the "Simple" model has an average error of 56.46°C, while each of the components has an error under 2°C. This is due to the fact that thermal errors are not necessarily linearly additive. A small mean error in a particular component of a thermal system can affect large changes in the thermal response of the system as a whole. This behavior can also be seen in the RC-compensated results.

Looking at long term transients (Default), the most important

| Component | Default Mean Error | RC-Compensated Mean Error |
|---|---|---|
| Mainboard | 0.27°C | 0.27°C |
| SOI | 0.85°C | 0.45°C |
| Interconnect | 1.64°C | 0.94°C |
| Package | 1.84°C | 0.30°C |
| **Simple** | 56.46°C | 8.19°C |

**Table 1: Component importance breakdown.**

components are the package and the interconnect (1.84°C and 1.64°C). For short term transients (RC-Compensated), the most important components are the interconnect and the SOI. This means that to accurately model temperature for long periods, we need to consider the package and the interconnect. At the same time, if we are interested in faster transients, we need to consider the interconnect and the need to model SOI versus Bulk silicon. In both cases, the mainboard seems to have a small impact; therefore, for the solution modeled, it is the least important component.

# 5. RELATED WORK

There are a variety of thermal models that have already been developed. These include HotSpot by Skadron et al [7], and Illiads-T [8]. It is not the aim of this paper to compare SESCTherm to these models. Rather, SESCTherm was developed for the purpose of exploring questions regarding the need to accurately model various modern technologies that are not currently modeled using these other software packages as of the time of this writing.

This work borrows from many other sources in the development of various material sub-models. The statistical interconnect distribution was determined following the work of Davis et al. [9, 10]. The mainboard model was developed following the work of Graebner et al. [11]. The package model was developed following the work of Ramakrishna et al. [2]. The Silicon-On-Insulator model was based, in part, on the work of Lin et al. [5] and others [6]. However, the bulk of the Silicon-On-Insulator model was based upon CMOS SOI, US Patent 6,975,003 [4].

Although a variety of other thermal models have been built, this work is not focused on an improvement to existing models. Rather, it is intended to highlight the need for more accurate thermal modeling – regardless of the model used. As such, the work here may be considered unique in that it is the first known study to include a robust validation of a thermal infrastructure using empirical data that is coupled with a detailed analysis for the modeling of new thermal features, including system-level modeling of Silicon-On-Insulator technology, interconnect density variation, package modeling, and mainboard modeling.

# 6. CONCLUSIONS

This paper has introduced a temperature modeling framework, called SESCTherm. The major contribution of the paper is to explore the thermal effect of several elements of a semiconductor device. This includes the thermal consequences of neglecting to model the system mainboard, device package, interconnect density distribution, and Silicon-On-Insulator technology. It has been shown that neglecting to model these elements can have dramatic consequences.

We show that, when attempting to accurately characterize the thermal behavior of modern semiconductor devices, it may be necessary to design thermal models that capture more details than has been previously believed to be required. Further, new technologies, including Silicon-On-Insulator technology, may exhibit different thermal behavior and may therefore necessitate the development of new material models.

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