

CURRICULUM VITAE

Martine Schlag

Current Position

Professor of Computer Engineering
University of California, Santa Cruz

Education

B.A. Mathematics 1978, University of California at Los Angeles
Mathematics, Graduate School, Yale University 1978-1980
M.S. Computer Science 1982, University of California at Los Angeles
Ph.D. Computer Science 1986, University of California at Los Angeles

Grants and Awards

University of California MICRO research grants, 1992-2002
National Science Foundation 3 year research grant:
“Routability-Driven Logic Partitioning for Multiple-FPGA Systems”
NSF REU Supplement, 1991
NSF Presidential Young Investigator, 1987
University of Washington Graduate School Research Fund, 1986
Graduate Woman of the Year 1986, (Association of Academic Women UCLA)
ARCO Doctoral Fellowship 1982-1985
National Science Foundation Graduate Fellowship 1978-1981
Martin Luther King Prize, (Phi Beta Kappa) 1978
Sherwood Prize in Mathematics 1978, (UCLA Mathematics Department)

Professional Service

General Chair: FPGA'02

Program Chair: FPGA'01

Program committee: FPGA'01, FPGA'00, FPGA'99, FPGA'98, FPGA'97, FPGA'96, FPGA'95 ACM
International Symposium on Field-Programmable Gate Arrays, Monterey, California, USA.

Associate Editor, *IEEE Transactions on Computers* 1992-1996.

Program Committee: Symposium on Integrated Systems, Seattle, Washington, March 1993.

Program committee: 11, 12, 13th Computer Arithmetic Symposium, 1993, 1995, 1997.

NSF RIA Panelist 1994

Selected Journal Publications

1. Pak K. Chan, Martine D. F. Schlag, Carl Ebeling and Larry McMurchie. Distributed-Memory Parallel Routing for Field-Programmable Gate Arrays. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Vol. 19, No. 8, pgs. 850-862, August 2000.
2. Jason Y. Zien, Martine D. F. Schlag, Pak K. Chan. Multi-level Spectral Hypergraph Partitioning with Arbitrary Vertex Sizes. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Vol. 18, No. 9, pgs. 1389-1399, September 1999.
3. Pak K. Chan, Martine Schlag, Jason Y. Zien. “Spectral-based k -Way FPGA Partitioning,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 5, pgs. 554-560, May, 1996.
4. Pak K. Chan, Martine Schlag, Jason Y. Zien. *Spectral K -Way Ratio-Cut Partitioning and Clustering*. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 9, pgs. 1088-1096, Sept, 1994.
5. Martine Schlag, Pak K. Chan and Jackson Kong. Routability-Driven Technology Mapping for LookUp Table-Based FPGAs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Vol. 13, N. 1, January 1994 pgs. 13-26.

6. Martine Schlag, Pak K. Chan and Jackson Kong. Empirical Evaluation of Multi-level Logic Minimization Tools for a Lookup Table-based Field-Programmable Gate Array Technology. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Vol. 12, No. 5, May 1993 pgs. 713-721.
7. Richard Anderson, Simon Kahan and Martine Schlag. Single-Layer Cylindrical Compaction. *Algorithmica*. Vol. 9, 1993 pgs. 293-312.
8. Pak K. Chan, Martine D.F. Schlag, Clark D. Thomborson and Vojin G. Oklobdzija. Delay Optimization of Carry-Skip Adders and Block Carry-Lookahead Adders using Multi-dimensional Dynamic Programming. *IEEE Transactions on Computers* special issue on Computer Arithmetic. Vol. 41, No. 8, August 1992 pgs. 920-930.
9. Y. F. Wu, P. Widmayer, M. D. F. Schlag, and C. K. Wong. Rectilinear Shortest Paths and Minimum Spanning Trees in the Presence of Rectilinear Obstacles. *IEEE Transactions on Computers* Vol. C-36 No. 3 pgs. 321-332. March 1987.
10. M. D. F. Schlag, E. J. Yoffa, P. S. Hauge, and C. K. Wong. A Method for Improving Cascode-Switch Macro Wirability. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* Vol. CAD-4 No.2 pgs. 150-155. April 1985.
11. M. Schlag, Y. Z. Liao and C. K. Wong. An Algorithm for Optimal Two-Dimensional Compaction of VLSI Layouts. *Integration, the VLSI Journal* Vol. 1 No. 2&3 (Oct. 1983) 179-209.

Related Conference Publications

1. Pak K. Chan and Martine Schlag. "Parallel Placement for Field-Programmable Gate Arrays," *FPGA '03: International ACM/SIGDA Symposium on Field-Programmable Gate Arrays*. Monterey, California, February 2003.
2. Pak K. Chan and Martine Schlag. New Parallelization and Convergence Results for NC: A Negotiation-Based FPGA Router. *FPGA '00: International Symposium on Field-Programmable Gate Arrays*. Monterey, California, February 2000.
3. Pak K. Chan and Martine Schlag. Acceleration of an FPGA router. *IEEE Symposium on FPGAs for Custom Computing Machines*, Napa, California, April 1997.
4. Aaron Ferrucci, Marcelo Martin, Tom Geocarlis, Martine Schlag and Pak K. Chan. A Field-Programmable Gate Array Implementation of a Self-Adapting and Scalable Connectionist Network. *FPGA '94: International ACM/SIGDA Workshop on Field-Programmable Gate Arrays*. Berkeley, California, February 1994.
5. Pak K. Chan and Martine Schlag. Architectural tradeoffs in field-programmable-device-based computing systems. *IEEE Workshop on FPGAs for Custom Computing Machines*, Napa, California, April 1993.
6. Pak K. Chan, Martine Schlag, and Marcelo Martin. BORG: A Reconfigurable Prototyping Board using Field-Programmable Gate Arrays. *FPGA '92: First International ACM/SIGDA Workshop on Field-Programmable Gate Arrays*, Berkeley, California, February 1992, pgs. 47-51.