

```
1 module control_logic(wheel,timeUp,PS,NS,reset_timer,bike);
2   input  wheel;
3   input  timeUp;
4   input  [4:0] PS;
5   output [4:0] NS;
6   output reset_timer;
7   output bike;
8   wire  IDLE, FW, BTW, RW, ERROR;
9   wire  Next_IDLE, Next_FW, Next_BTW, Next_RW, Next_ERROR;
10
11  assign IDLE  = PS[0];
12  assign FW    = PS[1];
13  assign BTW   = PS[2];
14  assign RW    = PS[3];
15  assign ERROR = PS[4];
16
17  assign NS[0] = Next_IDLE;
18  assign NS[1] = Next_FW;
19  assign NS[2] = Next_BTW;
20  assign NS[3] = Next_RW;
21  assign NS[4] = Next_ERROR;
22
23  assign Next_IDLE  = IDLE&~wheel | RW&~wheel;
24  assign Next_FW    = (IDLE|ERROR)&wheel | FW&wheel;
25  assign Next_BTW   = BTW&~wheel&~timeUp | FW&~wheel;
26  assign Next_RW    = RW&wheel | BTW&wheel;
27  assign Next_ERROR = ERROR&~wheel | BTW&timeUp&~wheel;
28
29  assign bike       = RW&~wheel;
30  assign reset_timer = FW&~wheel;
31
32 endmodule
33
```