Terman's method was used to evaluate the density of interface states in the MIS structures by calculating the difference in the slope between the experimental and theoretical surface potential-voltage dependencies. The analysis showed a low minimal interface state density D_{it} of 1×10^{11}cm^{-2} eV^{-1} in the AlN/GaN MIS structure. The interface state density was found to decrease when the surface potential varies from E_C to 1eV below the conduction band edge. The increase of the interface state density for energies below E_C – 1eV is attributed to measurement errors due to increased MIS leakage. The studies reported in this Letter show that good interface properties can be obtained from AlN/GaN heterostructures.

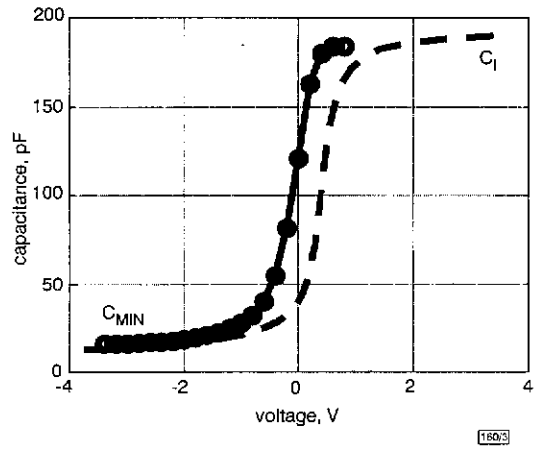

Fig. 3 *C-V characteristics of AlN/GaN MIS used to evaluate interface density of states of AlN/GaN heterojunction*

——— measured
- - - - calculated

In summary, AlN/GaN heterostructures using thin epitaxially grown AlN barrier layers have been investigated for the purpose of developing III-V-based MISFETs. C-V characterisation and Terman's method were used to demonstrate a low interface state density of the AlN/GaN interface. The high quality of the interface is confirmed by very high values of transconductance and current density obtained from HFETs fabricated on the AlN/GaN layers. These results indicate a high potential of AlN/GaN MISFETs for microwave power applications.

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References

1 SHEPPARD, T.S.: 'High power microwave GaN/AlGaN HEMTs on semi-insulating silicon carbide substrates', *IEEE Electron Device Lett.*, 1999, **20**, (4), pp. 161–163
2 EASTMAN, L.: 'GaN materials for high power microwave amplifiers', Proc. MRS Spring Meeting, 13–15 April 1998, pp. 3–7
3 WU, Y.F.: 'Short-channel $Al_{0.5}Ga_{0.5}N$/GaN MODFETs with power density > 3W/mm at 18GHz', *Electron. Lett.*, 1997, **33**, (20), pp. 1742–1743
4 SAUNIER, P., NGUYEN, R., MESSICK, L.J., and KHATIBZDEH, M.A.: 'An InP MISFET with a power density of 1.8W/mm at 30GHz', *IEEE Electron Device Lett.*, 1990, **11**, (1), pp. 48–49
5 ALEKSEEV, E., EISENBACH, A., and PAVLIDIS, D.: 'MOCVD grown AlN/GaN HFETs', 23rd Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE '99), Chantilly, France, 26–28 May 1999
6 EISENBACH, A., ALEKSEEV, E., and PAVLIDIS, D.: 'Growth and characterization of AlN/GaN HFETs', Ninth Biennial Organometallic Vapor Phase Epitaxy Workshop, Ponte Vedra Beach, Florida, 23–27 May 1999
7 BINARI, S.C., DOVERSPIKE, K., KELNER, G., DIETRICH, H.B., and WICKENDEN, A.E.: 'GaN FETs for microwave and high-temperature applications', *Solid-State Electron.*, 1997, **41**, (2), pp. 177–180

SiGe micro-cooler

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Thin film SiGe heterostructure coolers have been fabricated and characterised. Cooling by as much as 1.1K at room temperature and 1.6K at a substrate temperature of 70°C over a 3μm Si/SiGe superlattice barrier has been measured. This corresponds to cooling power densities of hundreds of watts per square centimetre.

Increased demand in the optical communications industry has led to many advances in semiconductor laser sources. These sources are efficient and operate at low threshold currents. As a result, heat dissipation is low (hundreds of milliwatts) and temperature dependent parameters can be stabilised with little cooling (< 20°C). Still, the low heat dissipation in conjunction with very small surface area (hundreds of square micrometres) results in a high heat flux density. Recent work on the miniaturisation of thermoelectric coolers (TECs), has shown the advantages of smaller coolers in these applications [1]. Thin film thermoelectric coolers that can be monolithically integrated with high speed, high power electronic and optoelectronic devices can improve the performance of these devices.

SiGe is a good thermoelectric material for high temperature applications [2]. It has been used for thermo-nuclear power generation in satellites for deep space missions. In this Letter we will describe the fabrication and characterisation of single-element thin film superlattice SiGe/Si coolers used for room temperature applications. Superlattice structures can enhance the cooler performance by reducing the thermal conductivity between the hot and cold junction [3], and by selective emission of hot carriers above the barrier layers [4].

The sample was grown in a Perkin-Elmer Si molecular beam epitaxy (MBE) growth chamber on a 125 mm diameter, (001)-oriented Si substrate, doped to 0.007–0.020Ωcm with Sb.

The structure of the sample consisted of a 3μm thick $Si_{0.7}Ge_{0.3}$/Si superlattice grown symmetrically strained on a buffer layer designed so that the in-plane lattice constant was approximately that of relaxed $Si_{0.9}Ge_{0.1}$. The buffer sequence, superlattice, and surrounding layers were doped to ~2×10^{19}cm^{-3} by first predepositing a 1/2 monolayer (ML) of Sb and then growing the various layers at a temperature of ~390°C. A supplemental Sb flux was provided at a cell temperature of 408°C throughout the growth in order to replenish the surface Sb concentration.

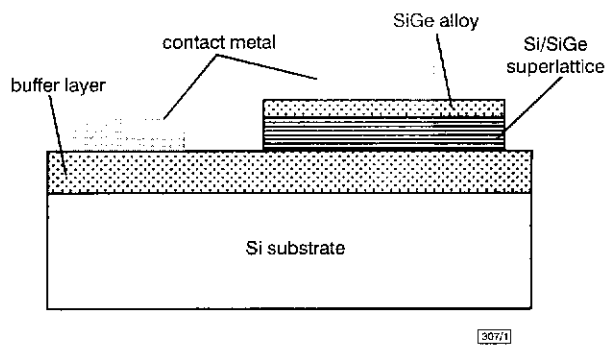

Fig. 1 *Schematic diagram of SiGe thin film cooler*

For the relaxed buffer layer, we used a 10 layer structure, alternating between 150nm $Si_{0.9}Ge_{0.1}$ and 50nm $Si_{0.845}Ge_{0.150}C_{0.005}$. Anneals were performed at 750°C for 10min after the growth of each $Si_{0.9}Ge_{0.1}$ layer, so that complete relaxation was obtained. Following the method of Osten *et al.* [6], the $Si_{0.845}Ge_{0.150}C_{0.005}$ layers were used to drive the dislocations into the Si substrate,

thereby resulting in a reduced threading dislocation density in the epitaxial superlattice layers. After the relaxed buffer sequence, another 150nm thick $Si_{0.9}Ge_{0.1}$ layer was grown at 390°C, followed by the 200 period, 5 nm $Si_{0.7}Ge_{0.3}$/10 nm Si superlattice. Finally, a 500nm thick $Si_{0.9}Ge_{0.1}$ layer was grown to cap the structure, followed by a 250Å thick, $10^{20}cm^{-3}$ $Si_{0.9}Ge_{0.1}$ contact layer.

The device structure is shown in Fig. 1. 3.7μm high mesas were formed using reactive ion etching down to the bottom layer of SiGe. To reduce the thermal resistance of the Si substrate and to achieve good heatsinking, the device backside was thinned down to ~100μm and metallisation was formed with titanium and aluminium. An SEM image of the processed devices is shown in Fig. 2.

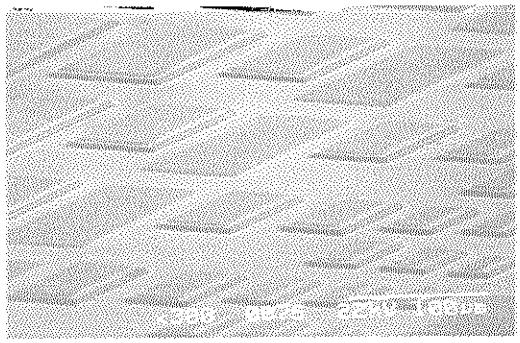

Fig. 2 *SEM image of processed SiGe micro-cooler devices*

Devices were tested from room temperature up to 70°C. Large devices (150 × 150 μm^2) were measured directly with probes, and small devices were mounted in packages and wire-bonded.

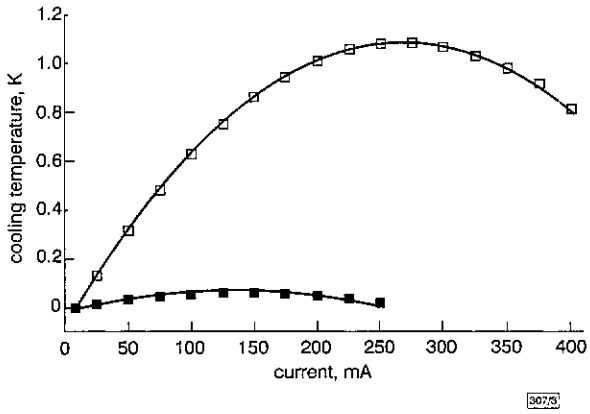

Fig. 3 *Cooling measured on top of thin film SiGe/Si cooler and on substrate*

Devices were measured with micro thermocouples
□ device
■ substrate showing Peltier effect

Fig. 3 shows the measured temperature on top of the device against current. The temperature is relative to the value at zero current. Despite the large thermal resistance of the Si substrate and the package on the hot side of the thin film cooler (estimated to be ~11.64K/W) and Joule heating in the wires connected to the cold junction, a net cooling of 1.1°C is observed on top of the device. This cooling over the 3μm layer corresponds to cooling capacities of the order of $100W/cm^2$. For comparison, the Peltier effect for the substrate is also illustrated in Fig. 4. The poor thermoelectric properties of Si are mainly due to its large thermal conductivity (of the order of 140W/mK).

Fig. 4 shows the measured cooling at various substrate temperatures. The device cools better at higher temperatures. A net cooling of ~1.6K is measured at 70°C. The reason for the improved performance is two-fold. First, the thermal conductivity of the barrier decreases at higher temperatures, and secondly, the thermionic emission cooling increases due to the larger thermal spread of carriers near the Fermi energy.

Various factors affect the overall performance of the device. These include the electrical and thermal conductivity in different layers, especially for the SiGe/Si barrier, selective emission of hot carriers above the superlattice barrier, the thermoelectric effect at the junction between different materials, package thermal resistance, and Joule heating in the wires connected to the cold junction, etc. Further experimental analysis and a 3D finite-difference heat equation solver [5] are under development to model the device performance. Based on the intrinsic properties of SiGe, integrated cooling by as much as 30–40°C is anticipated.

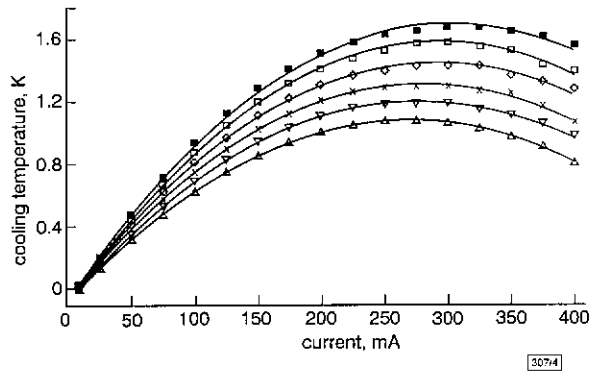

Fig. 4 *Measured cooling at various substrate (heatsink) temperatures*

■ 70°C
□ 60°C
◇ 50°C
× 40°C
▽ 30°C
△ 20°C

SiGe micro-coolers were fabricated and cooling up to 1.6K has been measured. Joule heating in the wirebonds connected to the cold junction, as well as the large thermal resistance of the substrate, are the major factors that hamper the device performance. Methods for improving the properties of these micro-coolers are now under consideration.

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References

1 SEMENYUK, V.A., PILIPENKO, T.V., ALBRIGHT, G.C., IOFFE, L.A., and ROLES, W.H.: 'Miniature thermoelectric coolers for semiconductor lasers', Proc. AIP Conf. 1995, **316**, pp. 150–153p. 150

2 VINING, C.B.: 'A model for the high-temperature transport properties of heavily doped n-type silicon-germanium alloys', *J. Appl. Phys.*, 1991, **69**, (1), pp. 331–341

3 LEE, S.-M., CAHILL, D.G., and VENKATASUBRAMANIAN, R.: 'Thermal conductivity of Si-Ge superlattices', *Appl. Phys. Lett.*, 1997, **70**, pp. 2957–2959

4 SHAKOURI, A., and BOWERS, J.E.: 'Heterostructure integrated thermionic coolers', *Appl. Phys. Lett.*, 1997, **71**, pp. 1234–1236

5 SHAKOURI, A., LABOUNTY, C., PIPREK, J., ABRAHAM, P., and BOWERS, J.E.: 'Thermionic emission cooling in single barrier heterostructure', *Appl. Phys. Lett.*, 1999, **74**, pp. 88–89

6 OSTEN, H.J., and BUGIEL, E.: 'Relaxed $Si_{1-x}Ge_x/Si_{1-y}Ge_yC_y$ buffer structures with low threading dislocation density', *Appl. Phys. Lett.*, 1997, **70**, (21), pp. 2813–2815